

A MANUFACTURABLE METHOD AND STRUCTURE FOR DOUBLE SPACER CMOS WITH OPTIMIZED NFET/PFET PERFORMANCE

Abstract

Disclosed is a method and structure where a first spacer is formed and an NFET is implanted, and then a second spacer is formed and a PFET is implanted. A dry nitride etch is then performed which selectively removes the second spacer, stopping selectively on an etch stop. This all dry removal process is more manufacturable than a wet etch, since it can be controlled to etch at a slower rate and it is not isotropic. This leaves a double nitride spacer on the PFETs and a single nitride spacer on the NFETs, giving the optimal spacer for each type of device. Furthermore, before silicide formation, the etch stop film on the nitride is removed, leading to a silicide edge very close to the gates for the NFETs, which is optimum for NFETs. The double nitride spacer on the PFETs prevents the silicide from getting too close to the PFET gate, which is optimum for PFETs.